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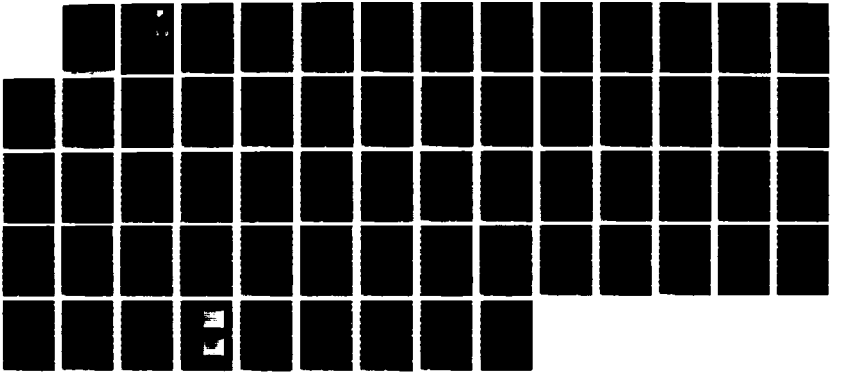

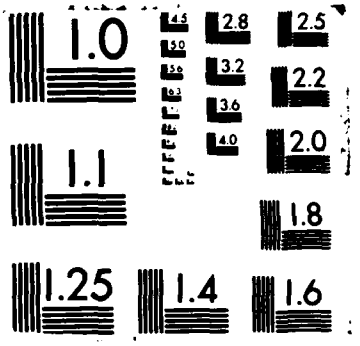
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OPTICAL CARRY ADDER

Aerodyne Research, Inc.

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We have constructed a hybrid electronic/electro-optic digital adder which uses an optical-carry for fully parallel operation. It adds two four-bit words at a data rate of 10 MHz. Electronic logic is used for summing the addend and carry bits, while the carries are generated optically. Ideally, this system reduces the number of gate delays associated with electronic addition of long addends, and has an execution time that does not increase with longer addends. The optical-carry (B. Arazi, Proc. IEEE 73, 162, 1/85) is based upon a multi-stage optical path, with sources which add light to the path if a carry is generated, and with modulators which allow light to pass if a carry is propagated, at the corresponding column of the addition. The signals which set the light sources and modulators are derived from the addends simultaneously, so the addition is completed as soon as detected light signals reach the summing logic. With small changes in the driving logic, the device operates as a parallel subtractor, with optical borrow propagation. Our breadboard system has six acousto-optic modulators (AOM's) as optical switches, with a single HeNe laser source.

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There is a 500 ns pipelined delay that is caused by the AOM's. The system data rate is limited by light loss through the carry path and by size effects. Such a system, if built in integrated optic form in GaAs, and with traveling-wave laser amplifiers as optical switches, should be able to add 32 bit words at 100 MHz.

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1. INTRODUCTION

Hybrid electro-optic systems, which combine the strengths of electronics and optics, may be useful for increasing the speed of digital computing and signal processing. All-optical logic devices[1,2] may eventually facilitate very high speed computation,[3] but for the near term, most logic functions will be best done with electronics. Electronic logic gates are inexpensive and convenient, consume small amounts of power, have fast switching times (< 1 ns) and are improving rapidly. We have been led to ask what can be done with optics to help relieve particular speed bottlenecks in digital computing, rather than attempting to replicate the functions that can be done easily with electronics.

One important strategy for increasing the speed of computing systems is to use parallel architectures. Optical techniques are often cited as a means of providing increased parallelism.[3,4] In digital addition, the carry operation is the main source of delay in execution. Recently, B. Arazi[5] proposed a method for parallel digital addition which uses an optical system for carry-bit generation and propagation. In this paper, we report the demonstration of an optical carry adder, which adds four bit words at a data rate of 10 MHz. This demonstration system uses the bulk optical technology of acousto-optic modulators, beamsplitters and HeNe laser source. This system serves to clarify the potential usefulness and limitations of the optical carry adder. Furthermore, we demonstrate how the optical carry adder concept can be extended to the operations of subtraction and multiplication.

This report is divided into two main sections, a short overview of the project followed by a set of appendicies that provide extensive detail on several aspects of the project. In the overview section, we will describe: the concept of the optical carry adder and how it increases the speed of digital addition; the construction and performance of the demonstration

optical carry adder; how the system can be optimized and what technology would be needed for an optical carry adder to be truly competitive with all-electronic systems.

This work was supported by the Department of the Air Force, Rome Air Development Center (RADC), Griffiss Air Force Base, and benefited from the interest and oversight of Dr. Vince Vannicola. This is the Final Technical Report for the second phase of Contract Number F30602-84-C-0130, covering the period of 26 August 1985 to 28 November 1986.

2. CONCEPT OF THE OPTICAL CARRY ADDER

2.1 The Problem of Digital Addition

In digital arithmetic, propagating carry bits from column to column is the primary feature which prolongs operations. Addition tends to be a serial operation, proceeding column by column, since the sum bit and carry bit at each column depend upon the carry bit from the previous column. The same can be said for subtraction, where borrow bits propagate from column to column. For simplicity, we will concentrate on addition in our initial discussions. (Extensions to subtraction and multiplication will be addressed in Section 2.3.) The serial nature of addition means that more time is required to add longer digital words. Significant increases in computation speed will result for systems that perform digital arithmetic in a fully parallel fashion. In such a system, the computation time would be independent of the number of bits.

The usual electronic solution to the serial nature of addition is to use Carry Look Ahead (CLA) circuitry,[6] which allows parallel addition for a limited number of bits. In the CLA, for each column added, all previous columns are checked simultaneously to determine if a carry is present. Only four logic gate delays are required for execution of the addition, with two layers of logic to determine the presence of carry bits in each column, and two layers of logic to form the sum of the two addend bits plus carry bit in each column.

With increasing number of bits, N, in the addends, the CLA approach leads to a large number of gates ($\sim N^2$), each with many inputs ($\sim N$). Since the number of inputs to a single logic gate is limited, for long digital words ($N > 8$) the CLA circuitry must be modified. The simplest approach to adding long digital words with CLA circuitry is to cascade four-bit CLA adders, so that four bits at a time are added in parallel. Commercially available[7]

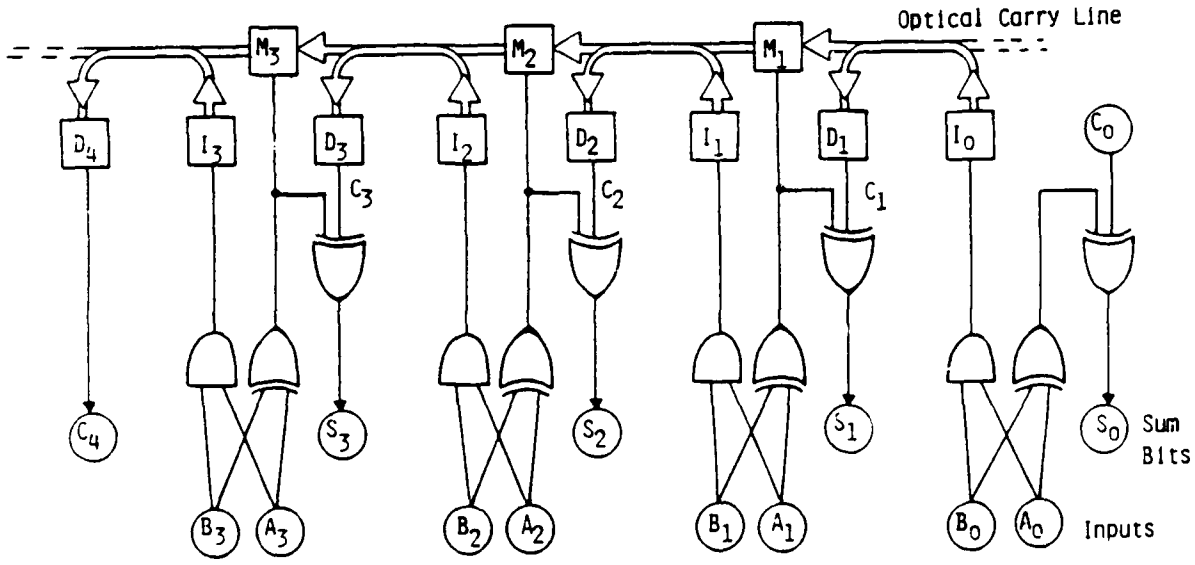
four-bit CLA adders on a TTL-family chip can produce the final carry output in ~5ns, so that for N-bits the addition delay is roughly (N/4) x 5 ns. A more sophisticated approach for long addends is to use more layers of logic in the CLA to combine the many inputs to each logic gate. In this way the growth in execution delay is only logarithmic. For example, if the maximum number of inputs per logic gate is 4, then just three layers of logic can be used for an equivalent 32-input gate. More delay may be incurred in this approach, however, since extra driver elements would be needed to drive the many logic gates in parallel.

Depending on the approach, the electronic CLA adders have a propagation delay that grows linearly or sublinearly with the length of the digital words added. The CLA circuitry has a great advantage over serial "ripple-carry" adders, but for long addends the CLA is not fully parallel and the propagation delay increases.

2.2 The Optical Carry Adder

The aim of the optical carry adder (OCA) is to produce a parallel adder with a propagation delay that does not increase as the number of bits increases. The OCA as presented by B. Arazi[5] is shown schematically in Figure 1. It consists of two basic segments, the electronic logic and the optical carry. The optical carry segment is a multi-stage optical path with a detector, modulator and light source in each stage, and as many stages as bits in the addends. Some element, such as a beamsplitter, allows injecting and sampling the light at each stage. Detected light indicates the presence of a carry bit at that stage. The electronic logic consists of an array of half-adders (AND and XOR gate in parallel), which drives the sources and modulators, plus final XOR gates that produce the sums.

The operation of the OCA is essentially parallel. The input data pulses go to the half-adders, whose outputs set all the light sources and modulators at once. The carry bits are generated as soon as the light in the carry-line is detected. The sum bits are then produced in parallel with the final layer



OPTICAL CARRY ADDER

Figure 1. Schematic of Optical Carry Adder

Electronic input bits are A_n, B_n. The optical carry line has modulators (M_n), sources (I_n) which inject light and detectors (D_n) which detect carry bits (C_n). Electronic logic (AND, XOR gates) drives the sources and modulators and produces the sum bits (S_n).

of electronic logic. The electronic logic for each stage does not look back at the earlier columns. The carry bits propagate optically, along paths determined by the modulators and sources.

The delays involved in addition with this system are due to the electronic logic, the process of light generation and detection, and the optical propagation time along the carry path. The electronic logic is only two layers deep, even for long addends, so the electronic logic delays are fixed (~2 ns). If the optical carry line is short enough, the optical propagation times can be as short as desired (< 1 ns). With fast modulators, sources and detectors, the carry line delays should be comparable to those of the electronic logic. Thus we expect that with an Optical Carry Adder, the delay in adding two 32 bit words could be as small as 5 gate delays, or about 5 ns. This is significantly less than the roughly 30 ns delay with all-electronic 32 bit adders. The highest operating frequency of an OCA will be limited by the electronic logic risetimes. Therefore, the maximum data rate for the OCA will be the same as for conventional electronic adders, provided the longer delays in the conventional adder are handled in a pipelined fashion.

2.3 Extension to Other Operations

With small changes in the driving logic, the Optical Carry Adder can function as an Optical Borrow Subtractor. If inverting gates are placed at the A_n inputs to the half-adders AND gates, and at the inputs to the modulators, then the system calculates A-B, with the presence of borrows signaled optically from column to column (see Figure 2). If we replace all the inverters that we use for subtraction with XOR gates, then we can convert the system from an adder to a subtractor with a single switch (that clamps all the second XOR inputs to logic-high).

The Optical Carry Adder may also be useful in fast digital multipliers. Digital Multiplication can be performed in two steps;[8,9] first form all the (N^2) cross products of all the bits of two N-bit words, and secondly add together the appropriately grouped columns of cross products. The first step

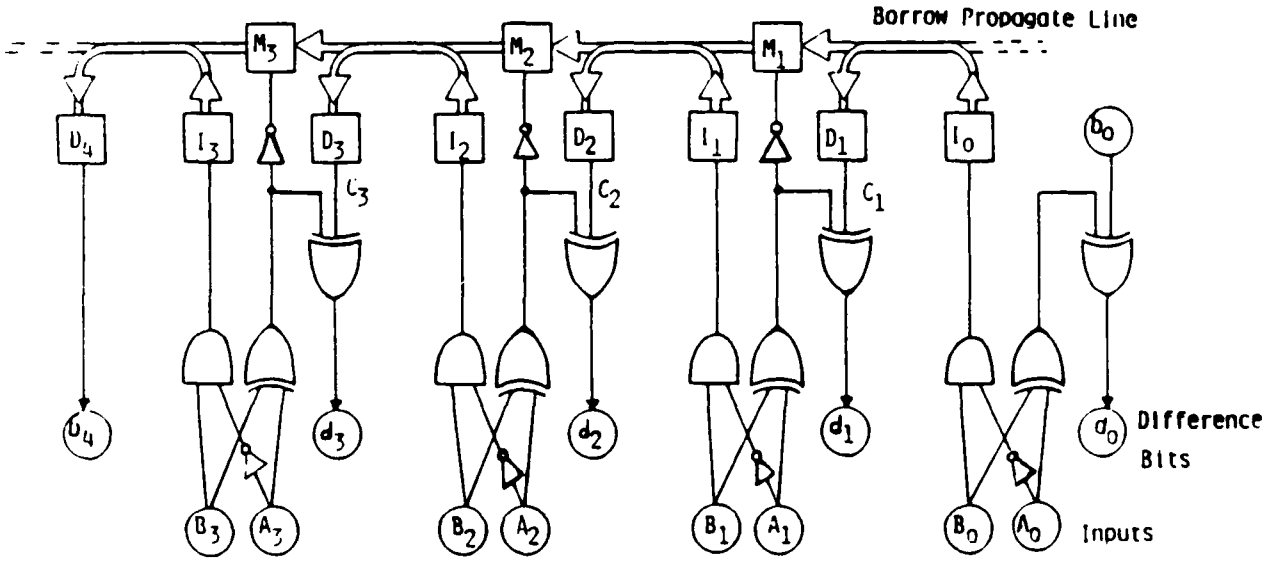


Figure 2. Optical Borrow Subtractor

can be done completely in parallel with an array of AND gates. Since the columns have up to N-elements, a fully parallel adder which performs the second step would be much more complex than for ordinary two-element addition. One can break up the N-element column additions into manageable size by first adding the column elements two at a time, and then adding pairs of these results in a staged system of adders. One would need roughly $\log_2 N$ stages and N-1 adders in order to combine the cross products in an N-bit multiplication. Since the Optical Carry Adder gives an advantage in propagation delay in executing additions, that advantage would be magnified where several stages of addition are used, such as in a multiplier.

3. THE DEMONSTRATION OPTICAL CARRY ADDER

3.1 System Design and Construction

In order to help clarify the issues concerning the performance and practicality of such a device, we have assembled a four-bit Optical Carry Adder with commercially available components. We use bulk optic technology in our optical system, which consists of acousto-optic modulators, beamsplitters and a HeNe laser source. We show a diagram of the system in Figure 3.

The optical carry path contains four modulators in series, so high modulator throughput is important. For this application we use acousto-optic modulators (AOM's) with the deflected beam as the modulator "on" state. These AOM's (TeO_2 crystals, manufactured by Newport E.O. Systems) have high deflection efficiency (~90%), reasonably fast risetimes (20 ns) and TTL compatible drive units. One drawback of an AOM for this application is the switching delay caused by the slow acoustic propagation ($4.2 \cdot 10^5$ cm/s for TeO_2), but this delay can be minimized by placing the laser beam close to the acoustic transducer. In our system, we operate with the laser at the acoustic focus for the greatest deflection efficiency, which results in delays of about 500 ns.

For the light sources, rather than use separately pulsed lasers, we use a single 5 mW HeNe laser with its output divided into beams that go through additional AOM's. This allows us to use the same switching waveforms and timing with the sources as with the carry path modulators. In the Arazi design, a four-bit adder requires four sources, but we reduce that to three by forming the final carry bit (C_4) with an extra step of electronic logic, in which the last detector signal (C_x) is combined with the final column addend bits (A_3, B_3), as $C_4 = C_x$ .OR. (A_3 .AND. B_3). This saves one AOM, and does not increase the propagation delay since the final carry is not used further.

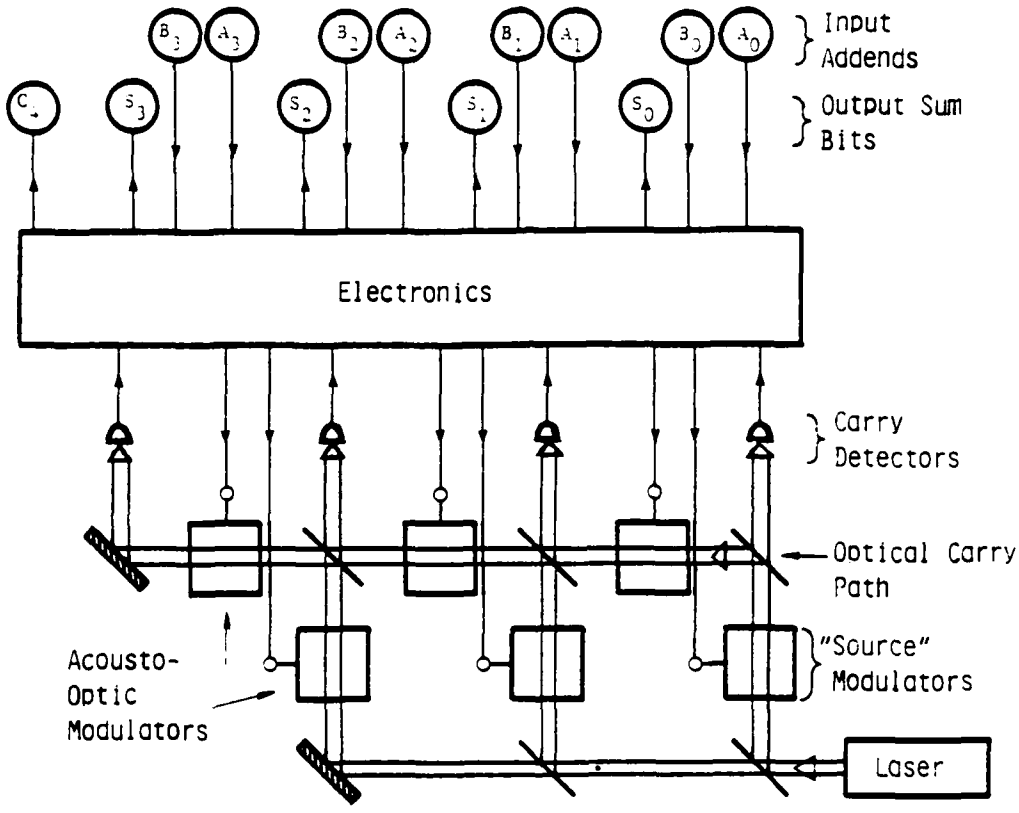


Figure 3. Diagram of Demonstration Optical Carry Adder

The light in the carry path is sampled with 50% beamsplitters which address Si-photodiodes (5 ns risetime). The detectors are followed by high speed amplifiers (600 MHz BW, 100 x gain) and fast voltage comparators with TTL outputs (9 ns delay). These detector/comparator modules provide TTL output pulses with input optical power of 30 μW, at switching speeds up to ~15 MHz.

The electronic logic system is built with fast-series TTL chips, with typical propagation delays of 3 ns. Since the optical carry signals are delayed several hundred nanoseconds by the AOM's, we include matching delays in the electronic logic. Hence all of the system delays are pipelined, and the clock frequency is not limited by the acoustic delays. The logic delay elements are shift registers, so the clock frequency must be adjusted so that an integral number of clock periods equals the acoustic delay. When operating with an acoustic delay of 500 ns, the clock frequency is a multiple of 2 MHz.

We provide more detail on the system design and construction in several Appendices. In Appendix A we discuss the limiting speed of the optical detection and how to maximize the speed by optimizing the beamsplitter reflectivities. Appendix B contains details of the optical system, and Appendix C contains details of the electronics.

3.2 Optical Carry Adder Performance

We have operated the demonstration Optical Carry Adder up to a clock frequency of 10 MHz, and it displayed the correct 5-bit sum of two 4-bit addends. We have observed the output with a set of five LED's and with an oscilloscope probe of the output channels. The input data pulses were derived from the system clock. We selected the numerical values for the addends with a set of switches. We had the option of dropping out a fraction (1/2, 3/4, 7/8) of the data pulses while maintaining the same clock rate, in order to simulate varying data streams (i.e., regular input words or all zeroes), as

well as to check that delayed logic pulses correctly aligned with the carry pulses. We operated with a carry delay of 500 ns, as determined by the point of maximum deflection efficiency in the AOM. This delay corresponded to five clock cycles at 10 MHz.

The operating frequency was limited by several factors that became important near 10 MHz. The AOM risetimes of 20 ns began to broaden the carry pulses. To some extent, this effect could be compensated for by trimming the logic pulse widths, but that would only work up to about 15 MHz. There was a variation in the arrival time of the carry pulses according to the different addends present. This addend dependent jitter in the carry pulses was due to the path length variation among the various carry paths, which could be as much as 1.8 meters in our system, giving temporal variations of 6 ns. The paths were relatively long in our system since the AOM's were mounted on baseplates 30 cm long, a length determined by the AOM focusing optics.

The variations in carry pulse length and arrival time were most apparent when both carry pulses and logic pulses were present at the final XOR gate, when the sum bit output should be completely cancelled. This would be the case if there was a carry from the previous column and one addend input to the column where cancellation should occur. Incomplete cancellation due to errors in overlap of carry and logic pulses caused short logic error spikes in the sum outputs. The error spikes could be suppressed (to below logic-high levels) so as not to affect subsequent processing by increasing the time constants of the output stage. This suppression would only work if the error spikes were narrow with respect to the total pulse width. At 10 MHz, the errors spikes were 10 to 20% of the total pulses, so we took that as the maximum operating frequency. The minimum light level in our system was 100 μW, so the maximum frequency was well below the limit imposed by photon shot noise. (See Appendix A.1).

Our test system shows that it is relatively easy to construct an Optical Carry Adder that works at modest speeds. The maximum frequency of our system is limited by the optical modulator risetimes and by path length variations.

The delay is dominated by the optical modulator acoustic delay. We present more detail on the system performance in Appendix D. The operation limits of our system are far below what might be achieved by using fast optical modulators in a compact, optimized design. We discuss some methods for building an OCA that would extend the performance of state-of-the-art electronic arithmetic in the following section.

4. STEPS TOWARDS A COMPETITIVE OPTICAL CARRY ADDER

4.1 Technology Requirements

We will now consider some of the technology issues that will affect the ultimate applicability of the Optical Carry Adder. The OCA has a potential advantage over electronic CLA adders in terms of reduced propagation delay for long digital words, (16-32 bits). The OCA would have the same maximum clock frequency as all electronic adders (provided the longer electronic adder delays were pipelined), and that frequency would be limited by the electronic logic risetimes. In an ideal OCA, the optical system would have risetimes and delays less than those of the electronic logic, so very fast light sources modulators and detector/comparators, as well as a short carry path would be needed.

We use here the example of a 32-bit adder operating at 100 MHz, with electronic logic risetimes and delays of 1 ns. In order to keep the addend-dependent jitter in the optical carry to below 1 ns, the total carry path must be less than 30 cm long (or 20 cm in glass, 14 cm in $LiNbO_3$). Thus, a 32 bit OCA could have only 0.4 to 0.9 cm per stage in the carry path, with one modulator and one beamsplitter per stage. This means that we need an optical technology that allows very compact devices. We will discuss below the use of integrated optic and fiber optic technology for this application. At the same time, we will discuss the optical modulator technology which must provide modulation bandwidths of at least 1 GHz.

A serious limitation on the data rate is presented by the integration time necessary for optical detection, especially with the large optical loss through a multi-stage path of modulators and beamsplitters. In order to get a good system bit error rate of 10^{-9}, one needs a signal-to-noise ratio of about 12, and for this SNR at 100 MHz, one needs a power of 0.2 to 0.5 μW (with a good Si-photodiode).[10] Thus if the source powers are 1 mW, then one can

afford a carry path loss of about 33 dB. That would imply a loss budget of only 1dB per modulator/beamsplitter in a 32 bit adder. Even if the input powers increase to 100 mW, the allowable loss per stage is less than 2 dB. See Appendix A.1 for details on the relationship between power and data rate.

4.2 Reflectivity Optimization

The reflectivities of the beamsplitters in the carry path can be adjusted to give the best utilization of the available optical power, which will yield the maximum system bandwidth. If we maximize the minimum power level that reaches any of the detectors, over any of the possible carry paths, then we will have the maximum system optical detection bandwidth. The set of reflectivities for the beamsplitters could refer equally well to the intensity coupling- coefficients for optical waveguide couplers.

We calculate the optimum set of reflectivities, R_j, as a function of the number of bits, N, and the average modulator loss, M, for the generic system show in Figure 4. the power, D_{nj}, at the n^{th} detector coming from the j^{th} source (of Power I_j), is given by:

$$D_{nj} = I_j M^{n-j} R_n R_j \prod_{k=j+1}^{n-1} (1 - R_k) \quad , \quad j < n-1$$

$$D_{n,n-1} = I_{n-1} R_n R_{n-1} M$$

$$D_{nn} = I_n (1-R_n) \quad .$$

The simplest method of optimizing the reflectivities is to make them all equal, then adjust their values so that the minimum D_{nj} is maximized. The minimum D_{nj} is then for the carry path with n = N and j = 1, or the path from the first source to the last detector, (with all the source intensities equal). The minimum is maximized with R = 2/N, so that the minimum power is given by:

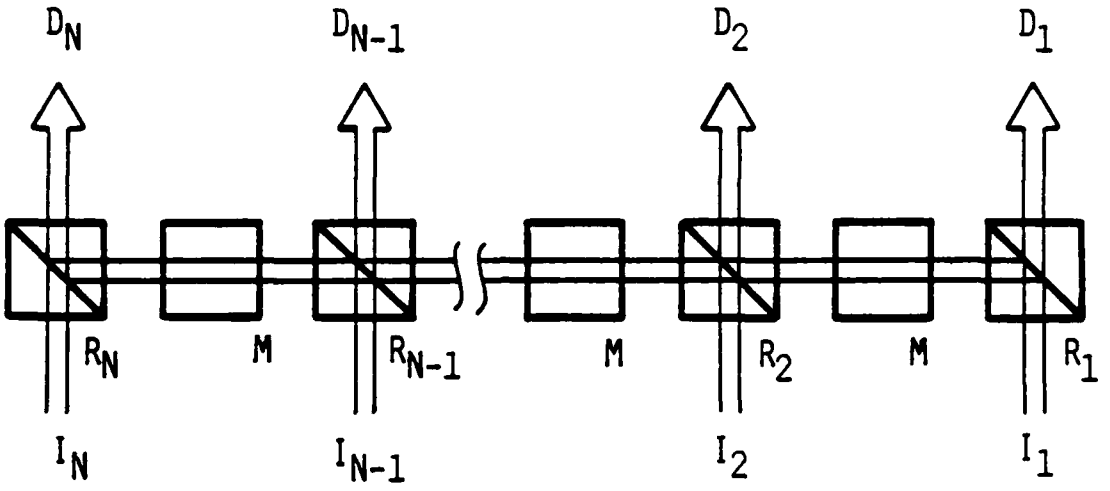


Figure 4. Generalized Carry Path, With Light Sources (I_j), Beamsplitters With Reflectivities R_j, Detectors (D), and Lossy Modulators (M).

$$D_{N1} = M^{N-1} \left(\frac{2}{N}\right)^2 \left(1 - \frac{2}{N}\right)^{N-2} \quad , \quad \text{with } I_j = 1 \quad .$$

We show some values of the minimum light level, (or system throughput), for some values of N and M in Table 1. The optimum R for a four-bit system is 50%, which is what we used in the demonstration OCA. The throughput falls rapidly with increasing number of bits and increasing loss. In a 32 bit system, the maximum modulator loss can be only ~ 0.02 dB, for a maximum system loss of 33 dB.

Having a set of reflectivities which are all the same does not give the best possible utilization of the optical power, since much more light would reach the detectors near the start of the carry line. We can increase the minimum light level by a factor of 3 to 9 by using a parabolic distribution of reflectivities, with the minimum R_j in the middle of the carry path and high R_j on the ends, i.e.

$$R_j = R_0 + B\left[j - \frac{(N+1)}{2}\right]^2 \quad .$$

We optimize the parabola coefficients, R_0 and B, to give the maximum-minimum D_{nj} for various number of bits and modulator loss. The results are shown in Table 2. Even though the throughput is better than with all-equal R_j, there is still a strong roll-off with the number of bits and the modulator loss. In this case, for 33 dB loss in a 32 bit system, the loss for each modulator can be only 0.25 dB.

We expect that the parabolic distribution of reflectivities gives nearly the optimum utilization of the optical power. We have performed calculations of reflectivity optimization using Monte Carlo techniques, i.e., where we repeatedly make small random changes in the reflectivities, then recalculate the minimum light level, and accept the changes if the minimum increases. Over many cycles, the reflectivity distributions converge to sets of values that are well described by the parabolic form shown above. We present more detail on the reflectivity optimization in Appendix A.2.

Table 1. Optimum Reflectivities and Minimum Light Level for All-Equal Set of Reflectivities, as a Function of the Number of Bits, N, and Modulator Transmission, M.

N	Optimum Refl.	Minimum Light Levels		
		M = 1	M = 0.9	M = 0.8
4	.5	$6.2 \cdot 10^{-2}$	$4.6 \cdot 10^{-2}$	$3.2 \cdot 10^{-2}$
8	.25	$1.1 \cdot 10^{-2}$	$5.3 \cdot 10^{-3}$	$2.3 \cdot 10^{-3}$
16	.125	$2.4 \cdot 10^{-3}$	$5.0 \cdot 10^{-4}$	$8.5 \cdot 10^{-5}$
32	.0625	$5.6 \cdot 10^{-4}$	$2.2 \cdot 10^{-5}$	$5.6 \cdot 10^{-7}$

Table 2. Optimum Reflectivities and Minimum Light Level for Parabolic Distribution of Reflectivities. Also Shown are the Optimized Parabolic Coefficients, R_o and B.

N	M	Optimum		Minimum Light Level
		Ro	B	
4	1.0	.40	.18	$1.8 \cdot 10^{-1}$
	0.9	.38	.20	$1.5 \cdot 10^{-1}$
	0.8	.35	.23	$1.3 \cdot 10^{-1}$
8	1.0	.20	.049	$4.6 \cdot 10^{-2}$
	0.9	.16	.052	$2.8 \cdot 10^{-2}$
	0.8	.13	.058	$1.6 \cdot 10^{-2}$
16	1.0	.093	.0060	$8.9 \cdot 10^{-3}$
	0.9	.055	.0062	$2.9 \cdot 10^{-3}$
	0.8	.027	.0069	$6.7 \cdot 10^{-4}$
32	1.0	.046	.0006	$2.0 \cdot 10^{-3}$
	0.9	.014	.0007	$1.6 \cdot 10^{-4}$
	0.8	.0025	.0008	$5.2 \cdot 10^{-6}$

4.3 Other Implementations - Integrated and Fiber Optic

The bulk-optic technology that we use in the demonstration OCA is unsuitable for a useful device that exploits the advantage of the optical carry concept. The AOM's that we use as carry-path and source modulators have risetimes that are too long and have relatively long switching delays. The large size of the AOM's leads to significant carry-bit jitter. Further, a serial arrangement of AOM's is difficult to align. These problems could be alleviated with guided wave optical technology, such as fiber optics or integrated optics.

Intergrated optic technology is attractive for this application since one can build a compact chip that has integrated modulators, beamsplitters (waveguide couplers), and possibly sources and detectors. Most of the integrated optic devices that have been described in the literature are made with lithium niobate ($LiNbO_3$).[11,12] This material has a high electro-optic coefficient and low loss waveguides can be readily formed in it. Electro-optic waveguide modulators in lithium niobate have been demonstrated with bandwidths in excess of 15 GHz.[13] One can envision a single-chip OCA in $LiNbO_3$ with detectors and sources (laser diodes) connected to the edges via optical fibers (See Appendix E). There are two drawbacks to using lithium niobate based integrated optics for an OCA, and these are the issues of loss and size. We estimate that there would be a loss of at least 6 dB per stage, due to propagation, bends and coupling effects.[12] That amount of loss is much higher than what could be tolerated in an adder for long digital words. A single stage of such a device may require 4 to 6 cm of propagation length, due to the very gradual bends that are used to minimize loss, as well as the length necessary for the electro-optic modulation to occur. Therefore, this device would not be as compact as desired.

An alternative to the passive material, lithium niobate, for an integrated optic OCA, is to use an active material, like gallium aluminum arsenide (GaAlAs).[11,12,14] In an active material, laser diodes, detectors, waveguides and even electronics can be combined on a single integrated wafer. The most important advantage that an active material offers for the OCA is the possibility of incorporating traveling-wave laser

amplifiers (TWLA) in the structure. Discrete TWLA's have demonstrated a single-pass optical gain of more than 25 dB, with an electrical modulation bandwidth in excess of 10 GHz.[15] The issue of loss becomes much less important with optical amplifiers in the carry path. In addition, the amplifiers could be used as the carry path modulators, so that separate electro-optic modulators would be unnecessary. If the amplifier at any stage in the OCA were turned off, then the propagation loss would effectively suppress the light in the carry path before the next stage. Such amplifiers with their high gain and high bandwidth could make very effective modulators. This type of device could be quite compact since the function of modulator and amplifier are combined, and the TWLA itself is rather short (~300 μm).

There are many technological problems involved in building an integrated opto-electronic OCA. The techniques for integrating a number of different types of devices, active and passive optical as well as electronic, are not yet mature. An intermediate step towards the fully integrated OCA would be to use fiber optic technology. An optical carry system could be built using discrete TWLA's linked with optical fiber directional couplers (which serve as beamsplitters). Most of the components for such a system are commercially available, including optical fiber-pigtailed laser diodes, detector modules and directional couplers. Since the TWLA is made with an anti-reflection coated laser diode, they are very similar to and might be adapted from commercially available super-luminescent diodes. Such a system might require about 3 cm per stage, so it would not be as compact as desired, but it would be shorter than what is possible with current passive integrated optic technology. A fiber-optic based OCA with amplifiers would not suffer from the problem of loss to nearly the degree of bulk optic or passive integrated optic systems.

5. CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

We have demonstrated the Optical Carry Adder concept in a four bit adder constructed with commercially available components. This has shown that it is relatively straightforward to construct an adder based on the scheme outlined by Arazi[5], and has helped clarify the system limits. The maximum data rate for our device (~10 MHz) is limited by several factors, including modulator risetime (~20 ns), addend dependent jitter in carry-bit arrival time due to the size of our system (~6 ns), and electronic delays (4-8 ns). Our demonstration adder has pipelined delays of 500 ns, which is mostly due to the acoustic propagation time in the acousto-optic modulators. This delay is not inherent to the optical carry adder concept, but reflects the choice of a modulator technology that allows high optical throughput and convenience of operation.

We have shown how the ultimate performance of an OCA is limited by light loss and by size effects. Even if the carry path reflectivities are optimized to make the best use of the available optical power, the light loss is severe in a multi-stage OCA. Small optical throughput increases the integration time necessary for optical detection, thereby limiting the maximum data rate. The most direct answer to the problem of loss appears to be to use traveling-wave semiconductor laser amplifiers as the carry path modulators, such that the carry signals are regenerated at each stage. An OCA with amplifiers might be fabricated on a single wafer of GaAlAs using the techniques of opto-electronic integration. An intermediate step to a fully integrated OCA would be to build a system with discrete laser amplifiers linked with fiber optic directional couplers. Since the maximum variation in the arrival time of the carry bits depends on the length of the carry-path, it is important to make the carry-path as short as possible (preferably less than 20 cm).

The Optical Carry Adder offers the potential advantage of a shorter propagation delay than is possible with an all-electronic adder, when adding long digital words (16-32 bits). The maximum data frequency would be limited by the speed of the electronic logic in the system. An OCA should be able to add 32 bit words at a data rate of 100 MHz, with a propagation delay of 5 to 10 ns, as compared to 30 to 40 ns for electronic adders.

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APPENDIX A

LIGHT LEVELS AND DETECTION SPEED

The operating speed of the Optical Carry Adder can be limited by the detection process if the light levels at the "carry" detectors are too low. Adequate integration time is required for low light level detection. In this section we will calculate the output light levels for the various detectors and for the various paths to the detectors. The maximum system detection speed is determined by the detector receiving the minimum power among all the detectors and all the possible optical paths to them. We will consider methods of setting the beamsplitter reflectivities so as to maximize the minimum light and thereby maximize the system speed.

A.1 Detection Speed

We now examine the maximum detection speed (maximum bandwidth) that can be used with a given optical power and a given maximum allowable error rate. This is a simple digital detection error rate calculation that we include for completeness.[10]

We examine the detection process at the photodiode, with noise due to dark current, thermal noise, and photon shot noise. We ignore sources of noise in later stages of the electronics, such as the amplifiers or comparators. The idealized detection system operates with some threshold, V_T, so that voltages above V_T register as "one" and below as "zero". The error probability per integration time (or, per bit, the Bit Error Rate, BER) is the probability that given an input "one" a "zero" is detected $[P_1(E)]$, plus the probability that given a "zero" a "one" is detected $[P_0(E)]$. By setting $P_1(E) = P_0(E)$, we have the minimum error rate, assuming ones and zeros are equally likely. We assume Gaussian noise statistics, so that:

$$P_0(E) = \int_{V_T}^{\infty} \frac{1}{\sigma_0\sqrt{2\pi}} e^{-x^2/2\sigma_0^2} dx$$

and

$$P_1(E) = \int_{-\infty}^{V_T} \frac{1}{\sigma_1\sqrt{2\pi}} e^{-(x - V_s)^2/2\sigma_1^2} dx \quad .$$

where σ_0 and σ_1 are the RMS noise voltages with no light and signal light present, respectively. The average signal level is V_s. These probabilities can be expressed in terms of the complimentary error function.

$$ERFC(x) = 1 - \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \quad ,$$

so that

$$P_0(E) = \frac{1}{2} ERFC \left(\frac{V_T}{\sigma_0 \sqrt{2}}\right)$$

and

$$P_1(E) = \frac{1}{2} ERFC \left(\frac{V_s - V_T}{\sigma_1 \sqrt{2}}\right) \quad .$$

Setting $P_0(E) = P_1(E)$ gives

$$V_T = V_s \left(\frac{\sigma_0}{\sigma_0 + \sigma_1}\right) \quad .$$

For a standard, low BER of 10^{-9},

$$P(E) = \frac{1}{2}\,\mathrm{ERFC}(X) = 10^{-9} \quad ,$$

so X = 4.24, or

$$\frac{V_s}{\sigma_0 + \sigma_1} = 6.0 \quad .$$

For a BER of 10^{-9}, one reads a signal-to-noise ratio of about 12.

Now, considering the noise sources, σ_d is the dark current noise, σ_T is the thermal noise and σ_s is the photon shot noise. We express all of these noise sources as RMS voltages. We will have

$$\sigma_0 = \left(\sigma_d^2 + \sigma_T^2\right)^{1/2}$$

and

$$\sigma_1 = \left(\sigma_a^2 + \sigma_T^2 + \sigma_s^2\right)^{1/2} \quad .$$

Using standard expressions for the noise sources,[10]

$$\sigma_d = R\sqrt{\frac{2qi_d}{\tau}} \quad , \quad \sigma_T = \sqrt{\frac{4kT}{R\tau}} \quad , \quad \sigma_s = R\sqrt{\frac{2q\ SP}{\tau}} \quad ,$$

with

R = load resistor (~50 Ω)
τ = integration time = 1/bandwidth
i_d = dark current
q = elementary charge
k = Boltzmans constant
T = absolute temperature (300 deg)
S = photodiode sensitivity (~0.4 A/w)
P = optical power incident

If we use numbers typical of good photodiodes, we can estimate the minimum integration time for a BER of 10^{-9}, as a function of input power. With; i_d = 10 nA, S = 0.4 A/w, R = 50 Ω, we have:

$$V_s = P \cdot S \cdot R = 20 \cdot P_{watts}$$

Then

$$V_s = 6 \cdot (\sigma_0 + \sigma_1) = \sqrt{\frac{6}{\tau}} \left\{\left[2R^2 q\, i_d + \frac{4kT}{R}\right]^{1/2} + \left[2R^2 q(i_d + SP) + \frac{4kT}{R}\right]^{1/2}\right\} ,$$

$$3.3\, P = \sqrt{\frac{1}{\tau}} \left\{1.84 \cdot 10^{-11} + \left[3.39 \cdot 10^{-22} + 3.2 \cdot 10^{-16}\, P\right]^{1/2}\right\} ,$$

$$\tau_{min} = (3.3\, P)^{-2} \left\{1.84 \cdot 10^{-11} + \left[3.39 \cdot 10^{-22} + 3.2 \cdot 10^{-16}\, P\right]^{1/2}\right\}^2$$

For a 100 MHz data rate, one would need an integration time of about 3 ns, which would give a minimum power of 0.2 μW. Due to extra noise in the following electronics, and sources that may be noisier than ideal thermal photon distributions, a realistic system should allow extra power. A

comfortable power level at 100 MHz would be ~0.5 μW. If one starts with a maximum source power of 1 mW, only 33 dB of optical loss can be tolerated in a 100 MHz system.

A.2 Optimizing Light Levels with Reflectivities

The reflectivities of the beamsplitters in the Optical Carry Adder can be adjusted to maximize the minimum light received by the carry detectors. In this section we describe in more detail, the methods used to optimize the reflectivities. Repeating the expression for the power at the n^{th} detector, coming from the j^{th} source, D_{nj};

$$D_{nj} = I_j M^{n-j} R_n R_j \prod_{k=j+1}^{n-1} (1 - R_k) \quad , \quad j < n-1$$

$$D_{n,n-1} = I_{n-1} R_n R_{n-1} M$$

$$D_{nn} = I_n (1-R_n) \quad ,$$

we will assume that all of the source intensities are equal to some maximum value, so we set $I_j = 1$.

a. The simplest method of optimizing the reflectivities is to make them all equal, then adjust their values so that the minimum light level is maximized. The minimum light level will be at the last detector, illuminated by the first source:

$$D_{N1} = M^{N-1} R^2 (1-R)^{N-2}$$

We find the optimum R by maximizing D_{N1}, with,

$$\frac{\partial D_{N1}}{\partial R} = M^{N-1} \{2R(1-R)^{N-2} - R^2(N-2)\ (1-R)^{N-3}\} = 0 \quad ,$$

so $R_{MAX} = 2/N$. Then we have

$$D_{N1} = M^{N-1} \left(\frac{2}{N}\right)^2 \left(1 - \frac{2}{N}\right)^{N-2} \quad ,$$

and

$$D_{nj} = M^{n-j} \left(\frac{2}{N}\right)^2 \left(1\frac{2}{N}\right)^{n-j-1} \quad , \quad j < n-1$$

In Figure A.1, we show the minimum light level as a function of the number of bits, N, and the modulator transmission, M. Even for low modulator loss, the light loss is severe for long digital words.

b. Our next method for setting the reflectivities was to use stochostic optimization. In this method, we imposed no biases as to the values of the reflectances, but repeatedly made small random changes in the reflectances, recalculated the minimum light level, and accepted the changes if the minimum increased. Over many cycles, the reflectances converged to sets of values that increased the minimum light levels by factors from 3 to 9, in the cases studied (N = 4, 8; M = 0.8, 0.9, 1.0). The reflectance sets arrived in this manner were well described by parabolas, i.e., with:

$$R_j = R_0 + B\left[j - \frac{(N+1)}{2}\right]^2 \quad ,$$

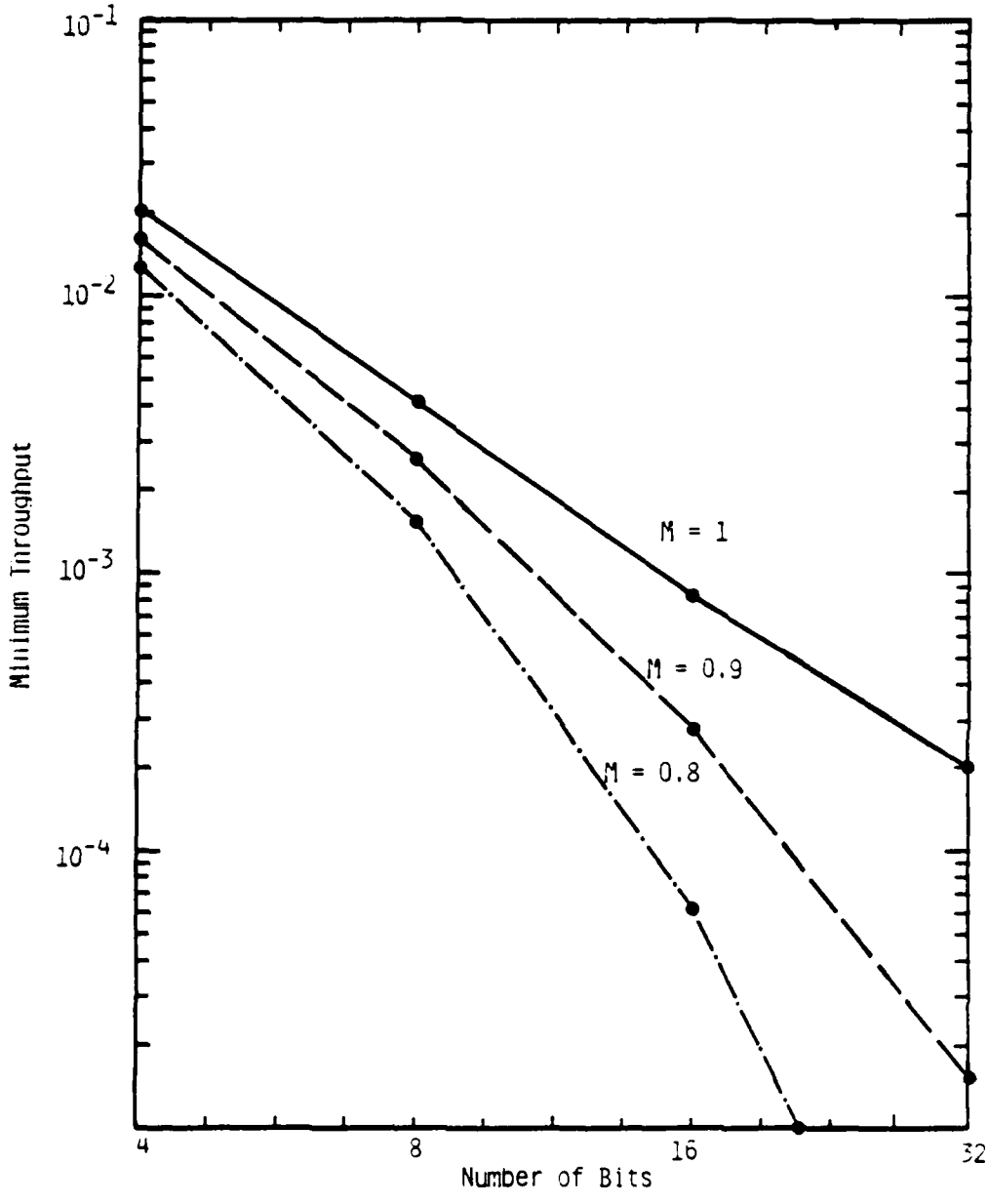


Figure A.1. Minimum Light Level at Any of the Detectors As a Function of Number of Bits (N), and Modulator Transmission (M), for Optimized All-Equal Reflectivities

with the low reflectances in the middle of the carry line and high values on the ends. This functional form for the reflectances has intuitive appeal, since higher reflection at the start of the adder sends more light downstream, and higher reflection downstream directs to the detectors more of the light already in the carry line.

With increasing number of bits, this method converges very slowly, for two reasons. First, the length of time necessary to calculate the minimum D_{nj} increases as the square of the number of bits. Second, the symmetrical parabolic distribution of R_j is strongly preferred in maximizing the minimum D_{nj}, so with random changes, far fewer sets of changes preserve the symmetry, when the number of bits is large. The amount of time needed by this method, as well as the apparently strong preference for the parabolic distribution led us to another method of optimization.

c. Finally, we used a parabolic distribution of reflectivities, and optimized the parameters R_0 and B in the equation shown above. This provided the highest values of minimum light, with short calculation times. In Figure A.2, we show the minimum light as a function of N and M. Again, the minimum light increased by a factor of 3 to 5, compared to the all-equal R_j method.

In Figure A.3, we show the sets of optimized reflectivities for 4, 8, and 16 bits, with modulator transmissions of 1.0 and 0.8.

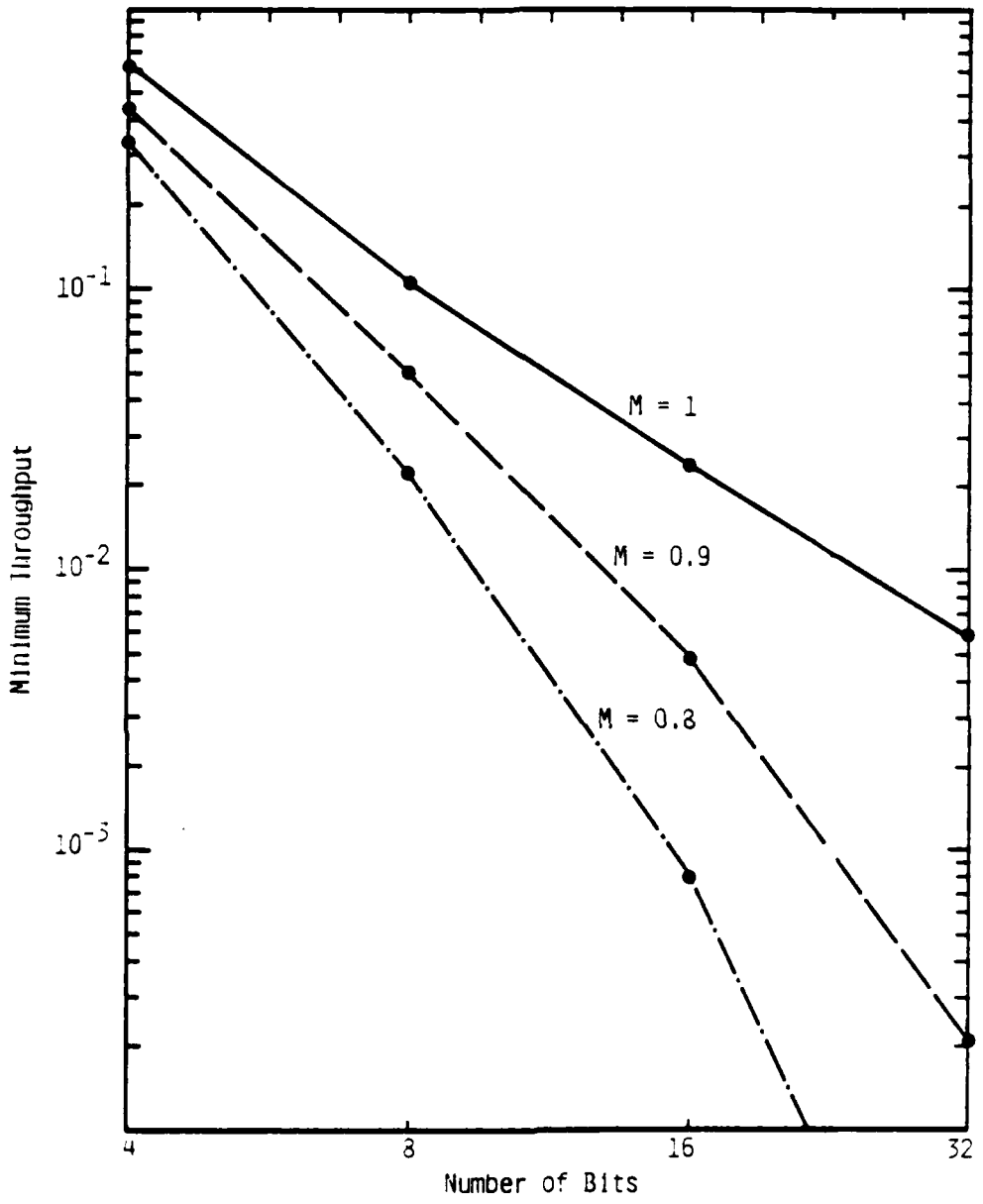


Figure A.2. Minimum Light Level At Any Of The Detectors for Optimized Reflectivities With Parabolic Distributions

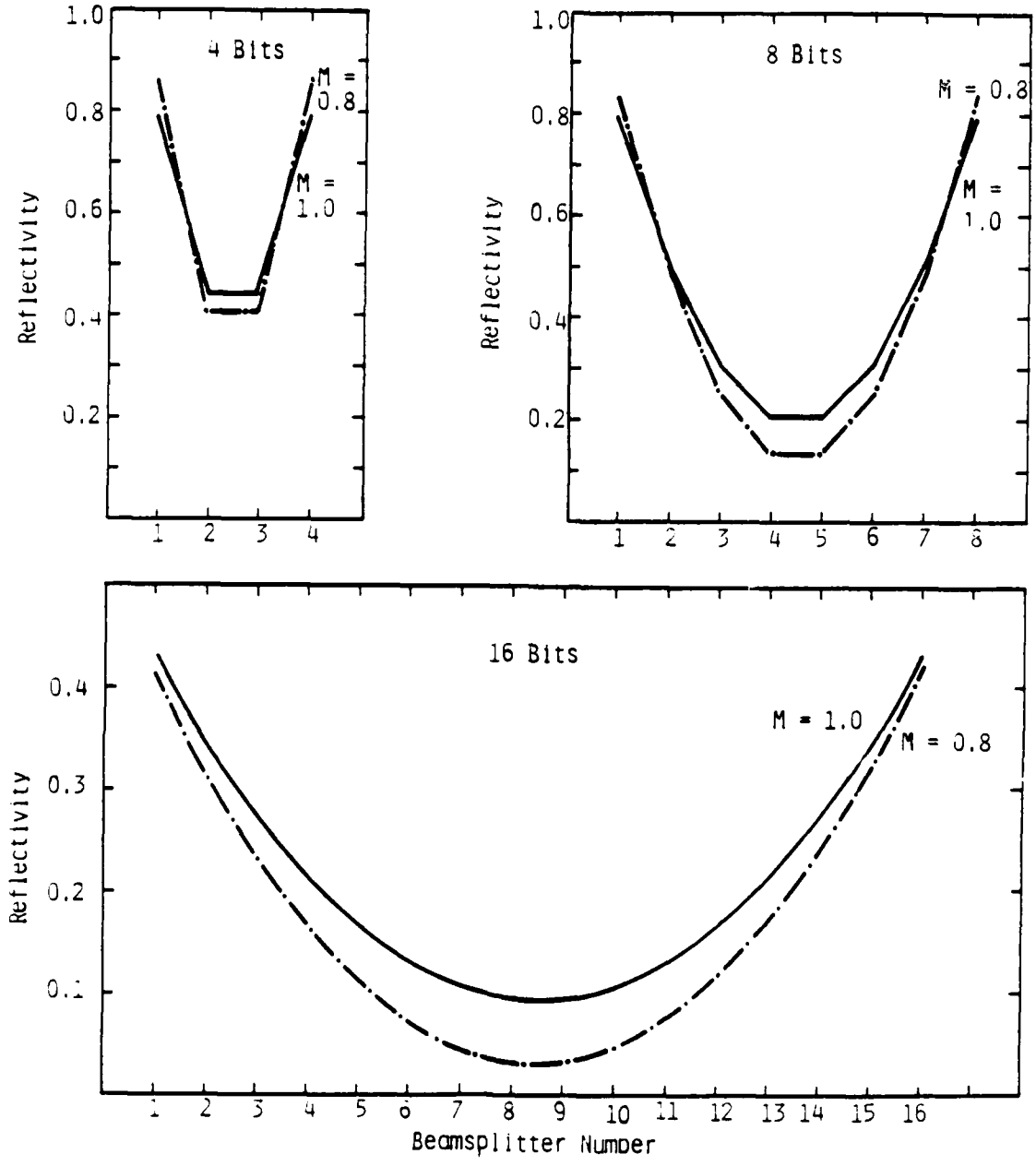


Figure A.3. Optimized Parabolic Distributed Reflectivities For 4, 8, 16 Bits

APPENDIX B

DETAILS OF DEMONSTRATION ADDER OPTICAL SYSTEM

B.1 Characteristics of Acousto Optic Modulators

The six acousto optic modulators that we used were manufactured by Newport, Electo-Optic Systems Group, Melbourne, FL. Some of the relevant specifications are given below.

Maximum deflection efficiency: 85 to 95%

Rise/Fall time (10% to 90%): 20 ns, with digital modulation

Transducer frequency and power consumptions: 250 MHz and 0.7 ±0.1 watt

Bragg angle: 0.018 Rad (~1.1 deg), for a deflection angle of 2.2 deg

Acoustic crystal: TeO_2 with refractive index 2.26, and acoustic velocity 4.22×10^5 cm/s

Focusing lenses: 16 cm focal length, giving a beam waist in the crystal of 87 μm (with a 1 mm diameter input beam)

One important piece of information that was not supplied by the manufacturer was the deflection efficiency as a function of the distance from the transducer to the beam waist. We would like to place the beam as close to the transducer as possible, to reduce the acoustic propagation delay (the delay between the RF wavetrain reaching the transducer, and the acoustic wavetrain reaching the beam waist). The acoustic delay is 240 ns/mm.

We made measurements of the deflection efficiency as a function of beam distance into the crystal, and show a typical curve in Figure B.1. We note that the zero position is only approximate. We also include in the figure, a measurement of optical switching delay vs. distance into the crystal. The efficiency falls off close to and far from the transducer with the optimum efficiency near a delay of 500 ns. There is a minimum delay measured to be roughly 110 ns. This minimum delay appears to be internal to the RF drive

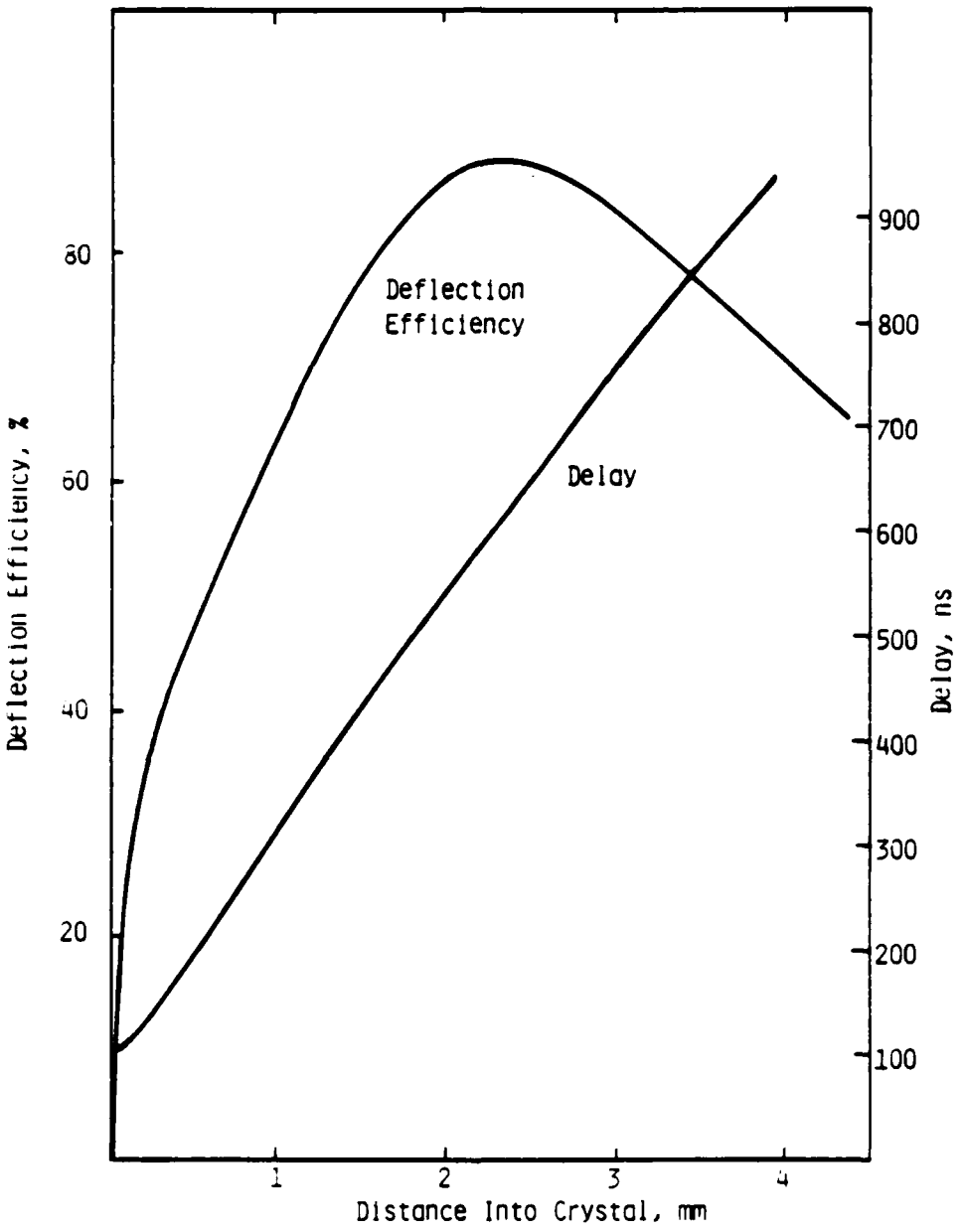


Figure B.1. Acousto-Optic Modulator Deflection Efficiency and Switching Delay As A Function of Distance From The Transducer To The Optical Focus

units. The peak efficiency near 2 mm into the crystal is due to acoustic focusing. The thickness of the acoustic beam was inferred by measuring the deflection efficiency vs. height of the beam in the crystal, for various distances from the transducer. The acoustic beam reached a minimum thickness, giving the maximum acoustic power density, near the depth of maximum optical deflection efficiency.

B.2 Optical System Setup and Alignment

In this section, we describe the general alignment requirements and problems for the Optical Carry Adder, as well as the specific techniques used to align the demonstration four-bit adder.

When the optical system of the Optical Carry Adder is properly aligned, the maximum amount of light reaches each detector for all the possible paths to each detector. In addition, the modulations which occur along each path must be synchronized. The condition of maximum optical throughput depends upon satisfying the Bragg angle for the beam going into each acousto-optic modulator (AOM), irrespective of its prior path. The synchronization condition is met by having the beams from all possible input paths focused at the same distance from the transducer in each AOM. Taken together, these alignment conditions mean that as each stage of the adder injects light into the carry path, the injected beam must overlap precisely, in angle and position, the beam defined by earlier stages. As the number of stages increases with increasing length of digital words to be added, the alignment becomes more difficult to establish and more sensitive to disruption. Angular errors in early stages propagate through the length of the carry path, causing increased positional errors towards the end of the system. The difficulty of alignment of a multi-stage bulk-optic system is an argument for the use of guided-wave technology (fiber optic or integrated optic) in a practical optical carry adder. In a guided-wave system, angular errors of injected beams cause only a one time loss of efficiency in coupling to the guided optical mode, without causing increased errors downstream.

We now describe the layout and setup of the optical system for the Reduced Four-Bit Adder. The basic system, shown in Figure B.2, consists of a HeNe laser, 3 mirrors (M), 5 beamsplitters (BS), 6 acousto-optic modulators (AOM), and 4 detectors (D). We don't show extra mirrors used to relay the carry-output beams to the actual detector locations (close to the electronics). We divide the system into two parts: 1) the three "source" modulators (labeled G0, G1, G2), with the lower row of beamsplitters and mirrors (BS4, BS5, M2); 2) the "carry-line" with three modulators (labeled P_1, P_2, P_3), and the upper row of beamsplitters and mirrors (BS1, BS2, BS3, M3). The overall beam layout is in the form of two adjacent squares, two feet on a side, with an additional arm (AOM-P_3) bent by M3 to fit on the 4 by 6 foot optical table. The size of this layout is dictated by the AOM baseplates, which measure 4.5 by 18 inches. The length of the baseplates is determined by the AOM focusing/collimating lens separation of 32.5 cm.

We use the light deflected by the AOM as the modulator "on" beam, since this beam has a contrast ratio of ≈1000:1, while the undeflected beam has a contrast ratio of only ≈10:1. using the deflected beams means that in each arm of the system containing an AOM, there is a bend in the optical path equal to twice the Bragg angle, or about 37 mrad (2 deg.). We set up the direction of the bends such that each deflected beam would enter the next AOM at the appropriate angle. The bends are shown exaggerated in Figure B.1.2.

One complication in the setup of the optical system is introduced by the beamsplitters, which are 0.25 inch thick glass, metal coated for 50% reflectivity on one side and AR coated on the other, with a 0.5 deg. wedge. At 45 degree incidence, the thickness of glass causes a lateral displacement in the transmitted beam of 1.5 mm, and the wedge causes a transmitted beam deflection of 0.43 deg. These deviations are easily apparent during the system setup, and make it necessary to mount some of the beamsplitters displaced from the table's rectangular bolt pattern.

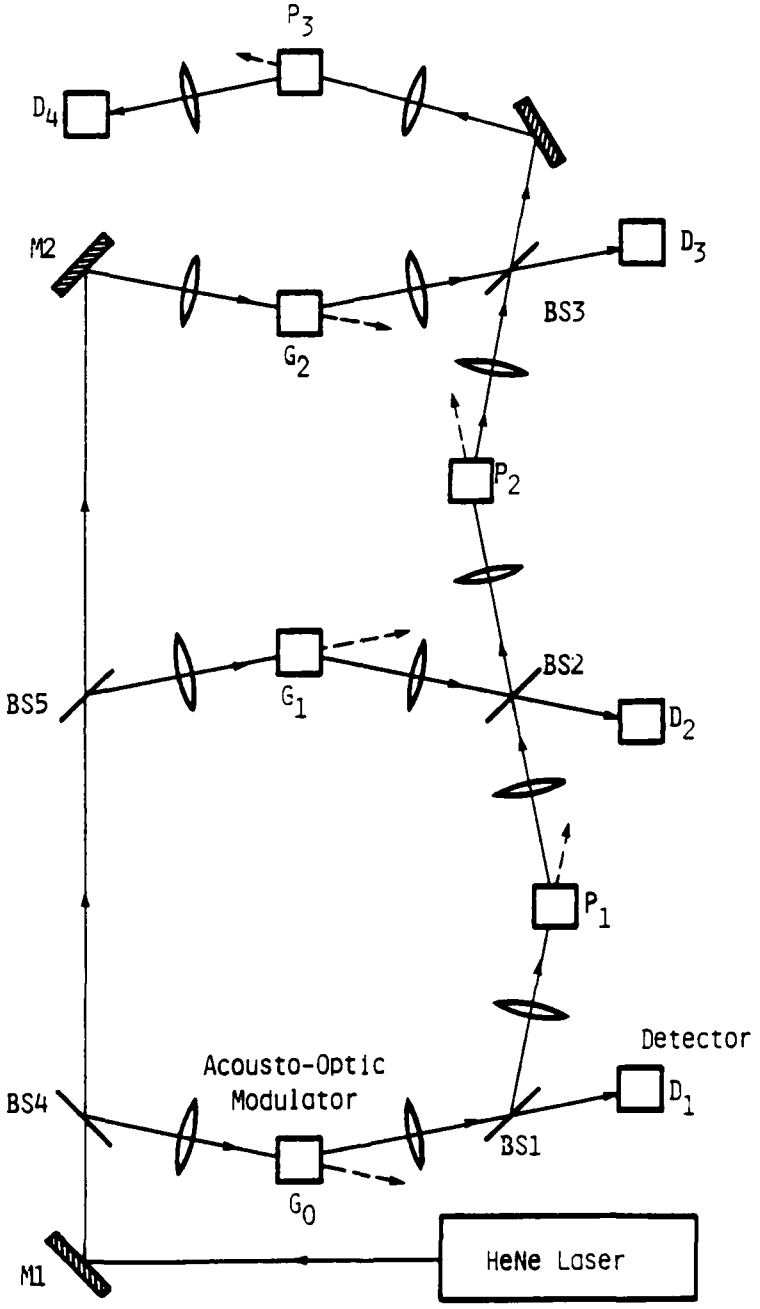


Figure B.2. Reduced Optical Adder Optical System

The steps in the setup and alignment are as follows:

1) Without the AOM's, set up the optical beams on a square pattern.

   1.1) Setup the input beam transport line (M1, BS4, BS5, M2) so that "source" arms (G0, G1, G2) are true along the table bolt lines. This leaves BS5 and M2 off the bolt pattern.

   1.2) Setup carry-line beamsplitters so that the carry line beam is as true along the table bolt line as possible. The beamsplitters are oriented so that the wedge induced deflections tend to counteract the lateral beam displacements.

   1.3) Verify accurate angular overlap in the beams from various paths by observing interference fringes at the detector positions.

2) Include AOMs in the order of G0, P_1, G1, P_2, G2, P_3.

   2.1) For G0, G1, and G2, tilt beamsplitters BS4, BS5, and mirror M2, to give Bragg angle beam inputs to the AOMs. Since the "source" AOMs provide the necessary bends in the beam paths, the top row of beamsplitters do not need to be adjusted for Bragg angle deflection.

   2.2) Adjust AOM input lens positions so that the Bragg angles are preserved, and beam heights don't change. Adjust output lenses similarly, with additional adjustment along the beam direction for a collimated output beam.

   2.3) Adjust AOM cell height and angle for maximum deflection efficiency.

   2.4) Fine tune BS angles to improve efficiencies for all AOMs at once.

3) Modulator synchronization adjustments.

3.1) Separately adjust the horizontal position of each AOM cell so that the rising edge of the detected light modulation is a standard delay after the driving pulse (typically 500 ns).

3.2) Synchronize carry path modulators, G0, P_1, P_2, P_3 so that when all of these are modulated at once the transmitted light pulse is not clipped on the leading or trailing edges.

3.3) Make fine adjustments in the source leg beamsplitters (BS5, M2) so that the injected light pulses, from G1 and G2, are synchronous with the light pulses injected by G0. At the same time, adjust the G1 and G2 longitudinal positions. These are the trickiest adjustments, since very small angular errors on the outputs of G1 and G2 lead to timing changes in the following AOMs.

With an input power of 5 μW, we detect the following powers at the detector positions D1, D2, D3, and D4, for the various optical paths indicated by the AOMs in the path.

Detector	Path	Power (mW)
D1	G0	1.16
D2	G1 G0+P_1	0.57 0.48
D3	G2 G1+P_2 G0+P_1+P_2	0.44 0.24 0.21
D4	G2+P_3 G1+P_2+P_3 G0+P_1+P_2+P_3	0.29 0.19 0.19

These powers correspond to an average AOM deflection efficiency of 85%. The delay in this case is 500 ns.

APPENDIX C

ELECTRONIC SYSTEM DESIGN

In this section we present design descriptions and schematics for the four-bit Optical Carry Adder electronics system. The system is built in three blocks; the word generator, the summing logic, and the detector/comparator modules. The system layout is shown in Figure C.1. The word generator provides any two four-bit digital words for addends. The summing logic operates on the addends, drives the optical modulators and completes the output sums when the carry signals arrive from the detector/comparator modules. The logic chips are all of the TTL family. Where possible, we use Fast-Schottky type chips (Motorola F74 series), which have typical propagation delays of 2 ns, for simple gates. The optical modulator drive units have TTL compatible inputs. The whole system is synchronized by a single clock, a square wave generator with adjustable frequency.

C.1 Digital Word Generator

The Digital Word Generator provides two four-bit digital words as addends. The values for the words, between 0 and 15 each, are selected by a set of 8 switches. The data rate is controlled by an external square wave clock. We can select a data rate of 1, 1/2, 1/4, 1/8 times the clock rate, with constant pulse width equal to the clock pulse width. This allows us to simulate rapidly changing data by alternating non-zero and zero inputs. Also, with the low duty cycle data, we can more easily check the proper synchronization of the logic board when delays of several clock cycles are used.

We show the schematic for the word generator in Figure C.2. The circuit begins with the clock input to the counter chip, 163A. The counter outputs with the following AND gates provide the output pulses at submultiples of the clock rate, but with the clock pulse width. Switches select the

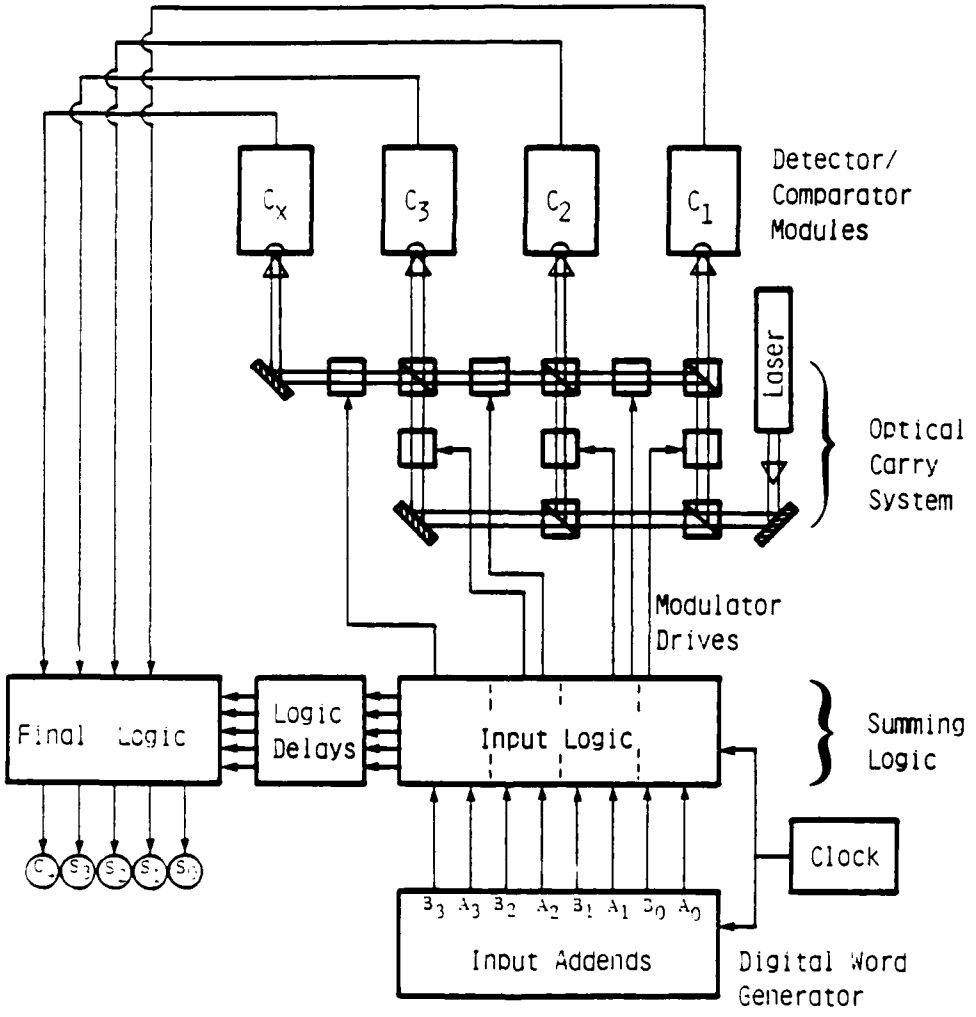


Figure C.1. Overall Electro-Optic System

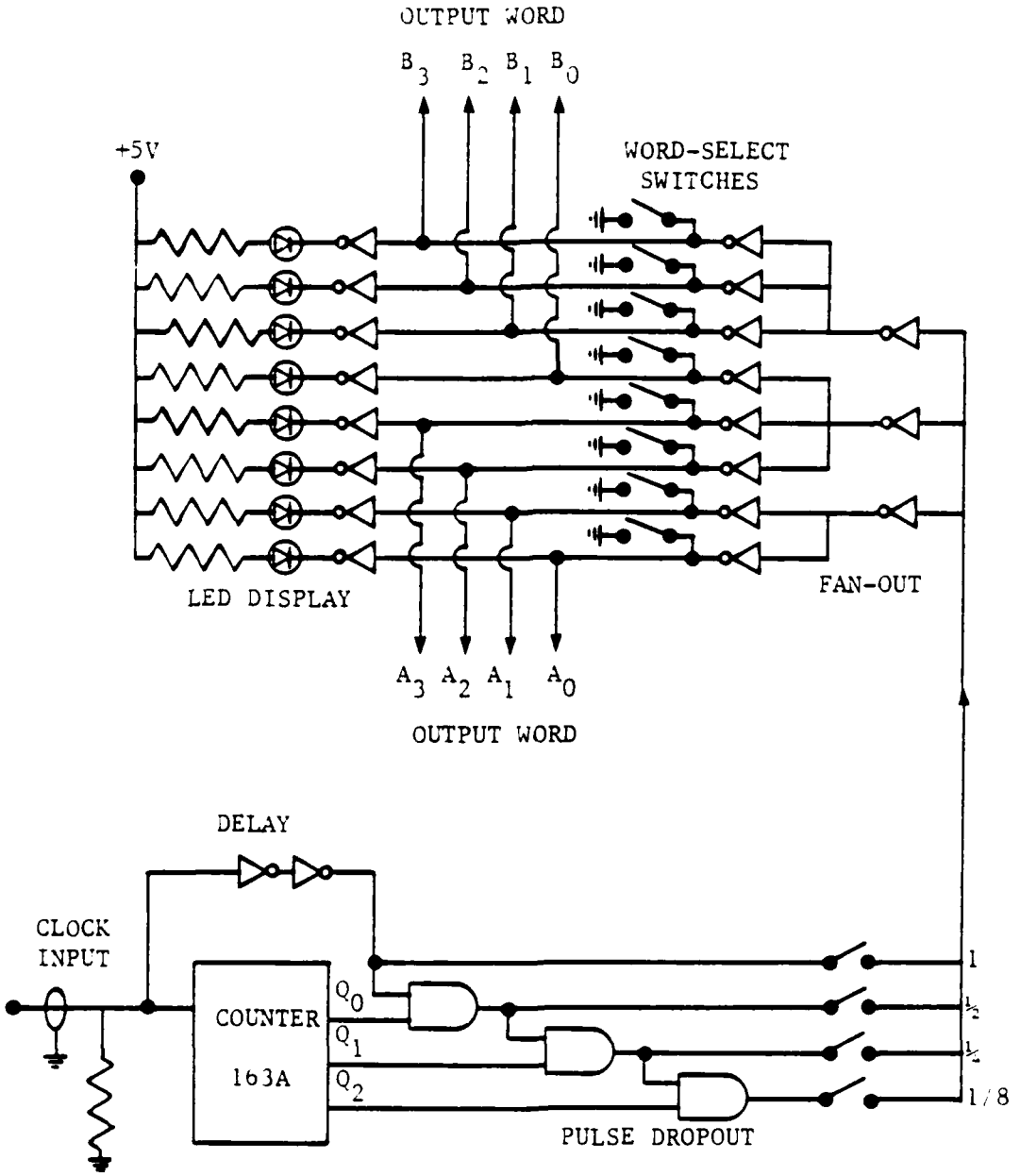


Figure C.2. Digital Word Generator

desired data rate, followed by inverters, to fan out to 8 data lines and 8 switches to select the active lines, for the two digital words. A set of 8 LEDs show the selected words. The circuit is constructed on a copper-clad board measuring 1.6 x 3.7 inches.

C.2 Detector/Comparator Modules

The detector/comparator modules convert the optical carry outputs into standardized TTL electronic signals. We constructed four nearly identical modules, each consisting of a photodiode (RCA C30808), two cascaded 10x amplifiers (Signetics NE520S) and a voltage comparator with TTL output (Advanced Micro Devices AM 686). We show the schematic in Figure C.3. Each module is built on a copper-clad board with a ground plane, and housed in separate boxes.

The photodiodes have a response of 0.4 A/W at 0.6328 μm wavelength, or 20 V/W into a 50 Ω load. The active area is 5 mm^2, giving a capacitance of 6 pF. The risetime into a 50 Ω load is listed as 5 ns. We provide each photodiode with a separate bias battery (42V). The input port of the NE5205 amplifier provides the 50 Ω load for the photodiode. The two cascaded amplifiers, of gain 10x each, provide a net gain of roughly 100x, giving a detector/amplifier sensitivity of roughly 2000 V/W. The specified bandwidth of the amplifiers is 650 MHz (-3 db point, 50 Ω load). The comparator which follows the second amplifier has a 1 kΩ load resistor, so the bandwidth of the detector/amplifier combination is substantially lower than 650 MHz. We measured the response at the comparator input, and got 2300 V/W at 1 MHz and 1440 V/W at 10 MHz. The risetime (25% - 75%) is 15 ns. This indicates an effective bandwidth of roughly 20 MHz.

The voltage comparators were the fastest available TTL compatible devices. The specified propagation delay was 9 ns, typical. We initially had the reference voltage set to 10 mV. The optical power for switching to a TTL-High output was approximately 30 μW at 10 MHz optical modulation rate.

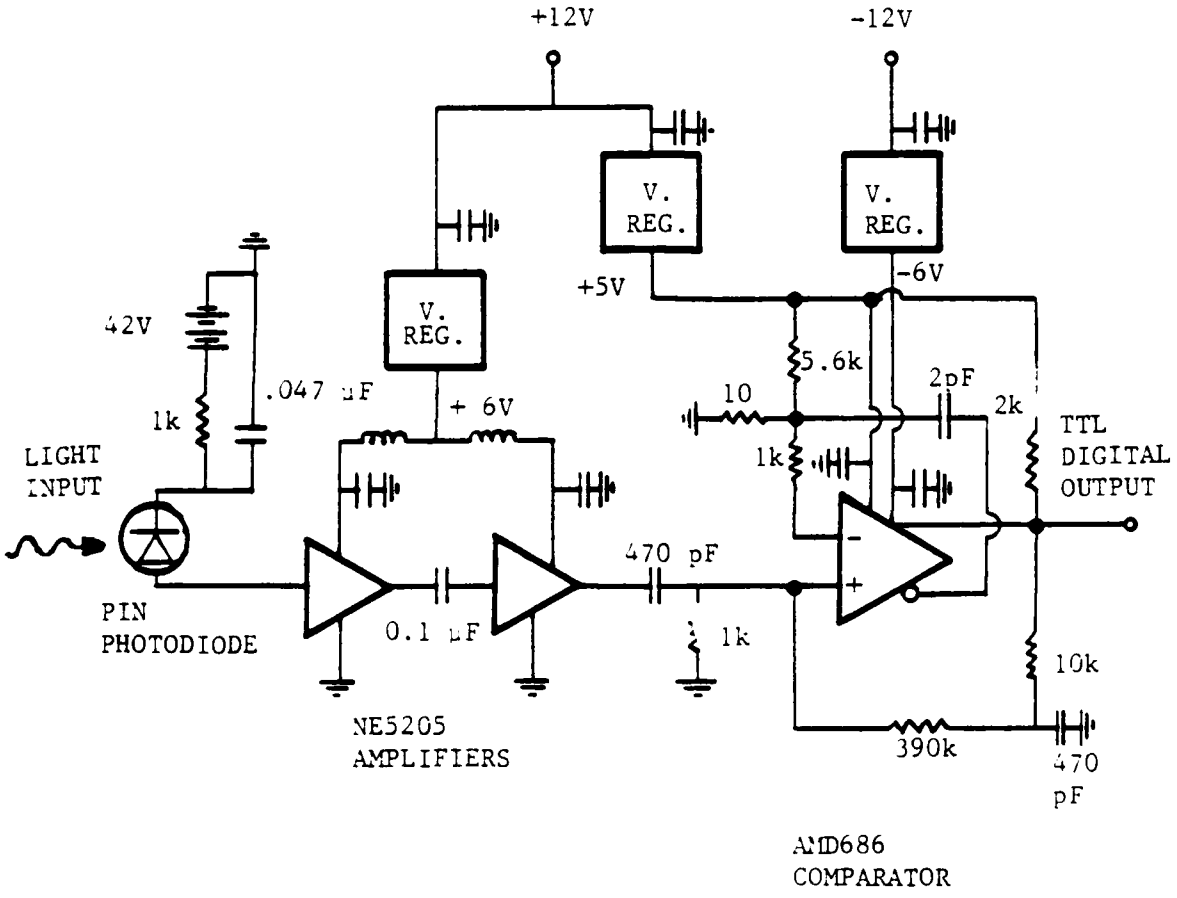


Figure C.3. Detector/Comparator Modules

This would give a voltage at the input to the comparator of roughly ±20 mV (A.C. coupling). Below that input power, the comparators tended to oscillate. Once all of the detector/comparator modules were connected to the electronic system, the presence of pickup between the comparators and other switching transients caused an increased tendency for comparator oscillation, so that we had to raise the reference voltage to 50 mV in three of the modules. The detector/comparator modules had voltage regulators and filter capacitors to reduce the effects of RF pickup.

C.3 Summing Logic

The summing logic schematic is shown in Figure C.4. The circuit functions as follows:

Each pair of input digits goes to a half-adder, which is an AND gate and Exclusive OR (XOR) gate in parallel. Each AND gate output drives a "source" AOM (G0, G1, G2), and each XOR gate drives a "carry-pass" AOM (P_1, P_2, P_3). Exceptions are made for the first XOR and last AND as described below. The XOR outputs also enter shift registers, which delay those pulses by an integral number of clock cycles, to match the optical carry delay. The delayed XOR pulses are combined with the optically generated carry pulses (from the detector/comparators) in a final set of XOR gates that produce the sum bit outputs. Since we do not provide a starting input carry for the first column (1's value), we do not drive a "carry-pass" modulator with the first XOR, and use that (delayed) XOR alone to produce the first sum bit. The final carry bit is produced by combining the last input AND result (delayed) with the last optical carry signal in an OR gate. This is a result of the "reduced" four bit adder design, which eliminates the need for one AOM. The sum outputs and final carry are displayed with a set of 5 LEDs.

Since the circuit uses shift registers (activated by the clock rising-edge) to delay the logic pulses to match the optical carry delays, the clock must run at a frequency that is an integer multiple of the inverse of the carry delay. With the carry delay set to 500 ns, the clock runs at 2, 4,

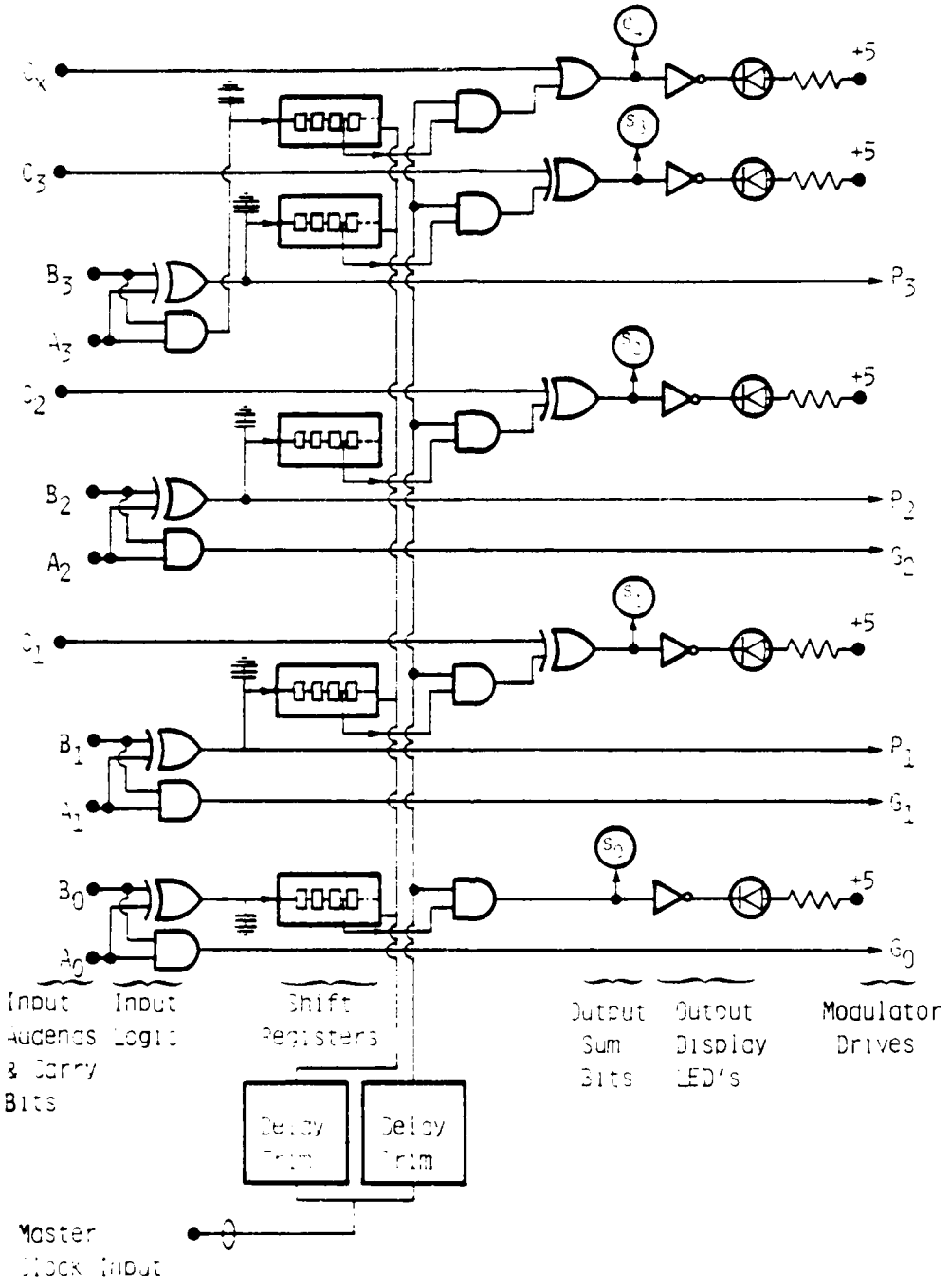


Figure C.4. Summing Logic

6 ...MHz. We made several adjustments in the circuit to allow operation up to 10 MHz. Small capacitors were added to the inputs to the shift registers to delay the data long enough for the clock to activate the inputs. The AND gates that shaped the outputs from the shift registers used a separate clock (derived from the main clock), with trimmed delays in the rising and falling edges to give better temporal overlap with the carry pulses.

The summing logic was built up in breadboard form only to allow us to make changes and adjustments in the circuit.

APPENDIX D

SYSTEM PERFORMANCE DETAILS

In this section we present a more detailed description of the performance of the final form of the demonstration Optical Carry Adder. In brief, the system operates up to 10 MHz, with a pipelined delay of 500 ns. It correctly displays the five digit sum of two four-bit addends, as observed either with a set of LEDs or with an oscilloscope probe of the output channels.

During the development of the system, the delay of 500 ns. was maintained from the start, while the maximum operating frequency was increased from 100 kHz to approximately 10 MHz, as we improved the electronics. The 500 ns delay was intrinsic to the AOMs when operating at peak deflection efficiency. We did not have sufficient optical power to sacrifice deflection efficiency in order to reduce the delay. Before we included the shift registers to delay the logic pulses to match the carry delays, the maximum system frequency was roughly 100 kHz (the frequency where delay induced logic error spikes were one tenth of the "true" logic pulse widths). After the shift registers were included, the system could operate at integral multiples of 2 MHz. We increased the frequency to 10 MHz by making small adjustments in the electronic logic board. The limit of 10 MHz was not a definite, hard limit, but was rather a point we chose where the difficulties of increasing the frequency, and the increase of irreducible errors were enough that further increases were not worthwhile.

There were two types of problems that we encountered as the clock frequency was increased, those electronic problems that could be solved by adjusting and trimming the circuit, and those problems that were essentially inherent. It was the inherent problems that ultimately limited the operating frequency. Those problems, described in the body of the paper, were: modulator risetimes of 20 ns broadening the carry pulses; and addend dependent

carry path variations causing variations in the carry arrival time. The purely electronic problems were of two types: RF coupling, and timing. These are described below.

The problem of RF coupling limited the optical sensitivity of the detector/comparator modules. If the detected optical signal was too close to the threshold voltage of the comparator, the comparator signal tended to oscillate. This behavior was much more evident when the full system was connected than when testing comparator modules independently. Most of the problem was due to the use of a temporary breadboard for building the logic board. If we had built up a stripline version of the logic board, then coupling problems would have been reduced. Short of that, we employed shielding and filter capacitors to reduce the problem to a manageable level.

As we increased the clock frequency, we had to adjust the logic timing and pulse widths. The shift registers were sensitive to the leading edges of the clock pulses, so we added small capacitors (50-100 pF) to the clock inputs as needed to add delays of 5-10 ns. We adjusted the pulse width in the clock that shaped the output of the shift registers so as to give the best overlapping pulse length with the carry pulses.

The most demanding operational condition was when both a carry pulse and a delayed logic pulse were present at the final XOR gate, such that the sum bit output should be completely cancelled. This would be the case if there was a carry from the previous column and one addend input to the column where cancellation should occur. We get this condition in the middle three sum bits if we add 15 + 1, so that all output digits except the last (value 16) should be logic low. We used this condition for fine adjustment of the clock frequency. We would adjust the frequency until we had the best dimming of the first four output LEDs, while adding 15 + 1. Differences in pulse width and arrival time between the carry pulses and delayed logic pulses caused short error output spikes where the cancellation in the final XOR was incomplete.

In Figure D.1 we show representative oscilloscope traces of various sum outputs when the system was running at 6 and 10 MHz.

Clock -

Delayed P_3 With 15 + 1 -

Carry C_3 With 15 + 1 -

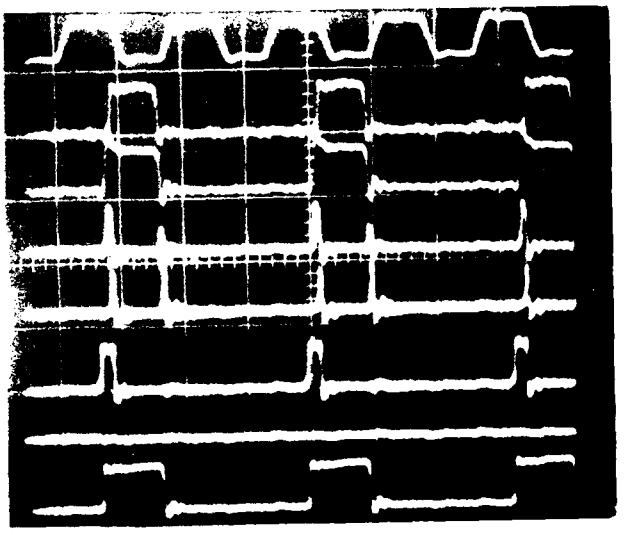
Sum S_3 With 15 + 1 -

Sum S_3 With 14 + 2 -

Sum S_3 With 12 + 4 -

Sum S_3 With 8 + 8 -

Sum S_3 With 4 + 4 -



Clock Frequency 6 MHz

Clock Frequency 10 MHz

Clock

Delayed P_3 With 15 + 1 -

Carry C_3 With 15 + 1 -

Sum S_3 With 15 + 1 -

Sum S_3 With 14 + 2 -

Sum S_3 With 12 + 4 -

Sum S_3 With 8 + 8 -

Sum S_3 With 4 + 4 -

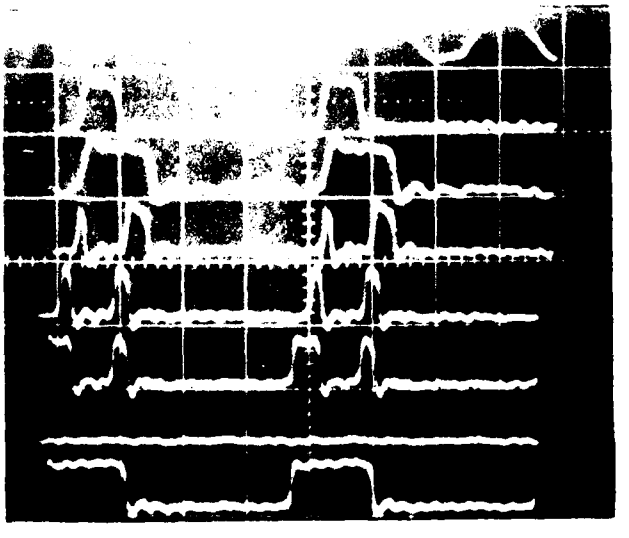


Figure D.1. Oscilloscope Traces of Various Sum Outputs

APPENDIX E

TECHNOLOGIES FOR A COMPETITIVE OPTICAL CARRY ADDER

In order to exploit the full potential of the Optical Carry Adder concept, one must build a system which has maximum frequency and delays limited only by the electronic logic. We described the requirements on such a system in the body of the paper. Here, we discuss in more detail two technologies that may be used in a practical OCA; the integrated optic chip and an optical fiber based system with traveling-wave semiconductor laser amplifiers.

In Figure E.1, we show a rough design for an integrated optic OCA that may be constructed in $LiNbO_3$ using electro-optic Mach-Zender interferometers as the modulators. These modulators have been shown to operate above 15 GHz.[13] With the double Y-branch construction of the Mach-Zender interferometer, their operation is relatively insensitive to fabrication variations (unlike directional-coupler type modulators). For each stage of the device, we show a Y-branch junction where light is added to the channel. Each junction has a coupling efficiency of 50%, and causes a 50% loss for light already in the channel. With sources and mirrors on the edges of the wafer, we can use a zig-zag optical path that gives a compact design. With the gradual bends that must be used to minimize loss, a length of 2 to 3 cm is used for each modulator, so without a folded path the device would be impractically long. With current technology, the loss per stage would be at least 6 db. [Propagation: 6 cm x 0.2 dB/cm = 1.2 dB; Bends : 9 x 0.2 dB each = 1.8 dB: Y-Branch input 3 dB].[11,12,14] The sampling of the carry light would introduce additional loss. Thus we can see that a conventional integrated optic OCA would suffer severe optical loss.

An alternative to the passive integrated optic form of the OCA is an optical-fiber based device with traveling-wave semiconductor laser amplifiers as modulators. These amplifiers have been shown to give in excess of 20 dB

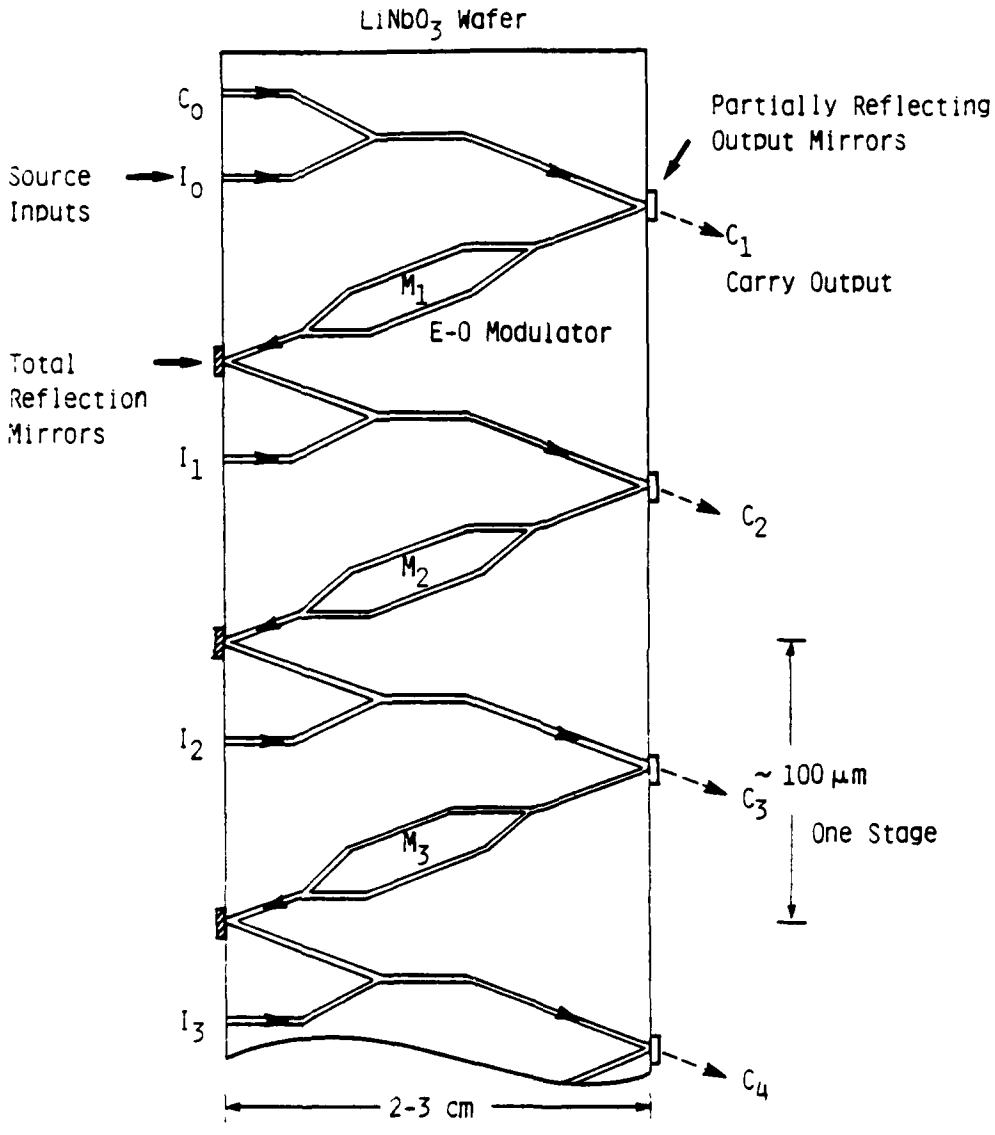


Figure E.1. Passive Integrated Optical Carry Adder

gain, with greater than 10 GHz modulation bandwidth.[15] With the signal regeneration that is possible with these devices, the loss per stage would be much less important. We show a schematic diagram of a system using fiber optic technology in Figure E.2. The beamsplitters would be replaced with fiber optic directional couplers. The laser diodes and detectors would be commercially available fiber-pigtailed devices. Such a design may be viewed as an intermediate step to a fully integrated version. The main technical challenges would be to adapt commercial laser diodes to function as traveling-wave amplifiers, and to achieve a compact design. Since a 32 bit OCA should have a total length of less than 30 cm to have carry bit timing variations less than 1 ns, there would be less that 1 cm allowed for each stage of the device. In order to use a semiconductor laser diode as a traveling -wave amplifier, both ends are anti-reflection coated and pigtailed to fibers. Very similar devices are already available commercially as super-luminescent diodes, which are AR coated but have fiber pigtails on just one end.

An approach that is a hybrid of the two techniques mentioned above offers the best hope for a practical optical carry adder. If one uses an integrated optic format in a semiconductor material such as GaAs, then one can combine sources (lasers), detectors and traveling-wave amplifiers all on the same substrate. Thus, a compact, rugged high speed device all on one chip could be realized with a minimum of hand-assembly. The field of integrated opto-electronics is moving ahead rapidly, so that such a device should be practical in the near future.

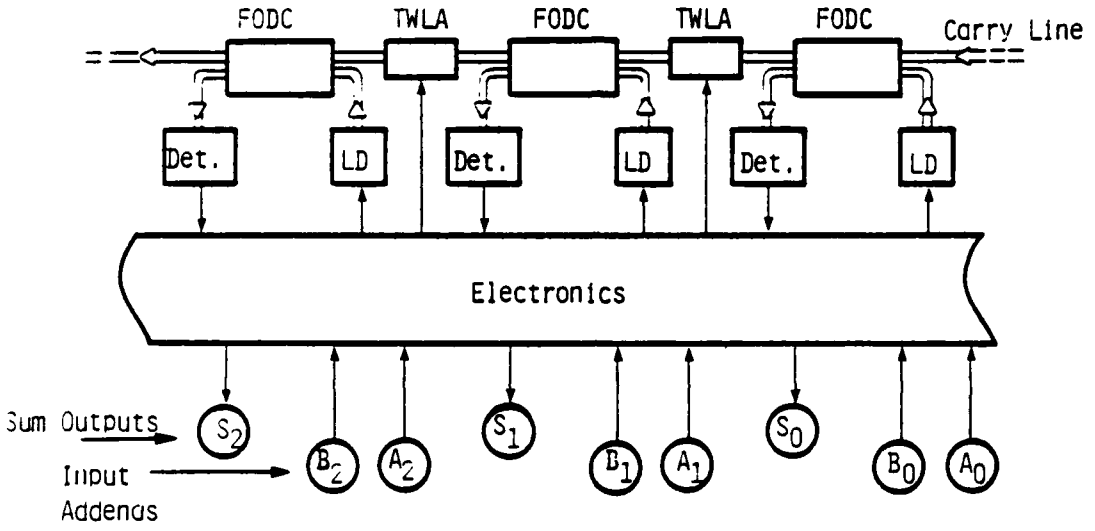


Figure E.2. Fiber Optic Technology Optical Carry Adder

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